Logic Operations of Chemically Assembled Single-Electron Transistor

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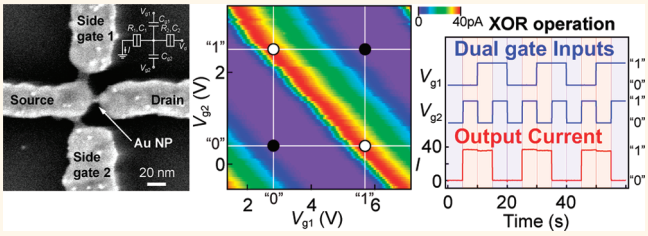
ABSTRACT



Double-gate single-electron transistors (SETs) were fabricated by chemical assembling using electroless gold-plated nanogap electrodes and chemisorbed chemically synthesized gold nanoparticles. The fabricated SET showed periodic and stable Coulomb oscillations under application of voltages of both gates. The sole SET also exhibited all two-input logic operations—XOR, XNOR, NAND, OR, NOR, and AND—with an on/off ratio of 10^2. This demonstrates the potential of chemical assembling to give highly stable SETs exhibiting all logic operations.

KEYWORDS: single-electron transistor · bottom-up process · self-assembly · nanoparticle · nanogap electrode · logic operation

Nanodevices such as single-electron transistors (SETs) have been studied extensively because of their potential low power consumption, high charge sensitivity, and multigate logic operation.[1−7] Tucker proposed the replacement of field effect transistors (FETs) with SETs in complementary-type logic gates,[8] where a logic gate composed of SETs would be smaller in size than a logic gate composed of the same number of FETs, owing to the small size of the individual SETs. The total number of SETs required for the logic operation can be decreased even further if the following beneficial features of the SET are considered: (1) the SET current oscillates as a function of the gate voltage and (2) in a double-gate SET, the phase of Coulomb oscillation shifts as a function of a linear combination of the two gate voltages. On the basis of these features, it would be possible to achieve the exclusive OR (XOR) gate operation of a single SET with a double-gate structure by using silicon technology[9−11] or carbon nanotubes (CNTs);[12] this is contrary to the case of a complementary-type XOR gate composed of 16 FETs. However, SETs have double-barrier tunneling junctions with Coulomb islands and gates, and therefore, there is a high demand for establishing methods for fabricating SETs that would give a precise device structure and have high process yield and high stability. Chemical assembling is a candidate method for fabricating nanodevices with precise structures on a subnanometer scale. Recently, we fabricated SETs in parallel composed of electroless gold-plated nanogap electrodes and chemisorbed chemically synthesized gold nanoparticles (NPs) by chemical assembling.[13−15]

In this paper, we demonstrate stable XOR and not exclusive OR (XNOR) operations of the chemically assembled SET with double side gates. We also demonstrate NOR, AND, OR, and NAND operations of the SET. Finally, we discuss the effectiveness of chemical assembling for the fabrication of the SETs in terms of achieving ideal SET properties and structure.

Figure 1a shows a scanning electron microscopy (SEM) image of fabricated SET with two side gates. A schematic illustration of a fabricated SET is shown in Figure 1b. White bright spots represented as decanethiol-protected Au NP[16] (core diameter of 6.2 ± 0.8 nm) and single Au NP was chemisorbed *via* decanedithiol[17,18] between electroless gold-plated nanogap electrodes,[19] which worked as a Coulomb island of SET. Double-gate electrodes were capacitively coupled equally to the Coulomb island, which is located in the center of side gate 1 and 2 electrodes.

RESULTS AND DISCUSSION

We characterized the electron transport properties of the fabricated SET under the

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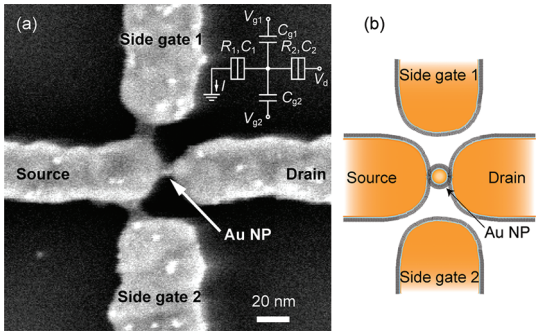

Figure 1. (a) SEM top-view image of chemically assembled double-gate SET comprising gold nanogap electrodes and a gold nanoparticle. Equivalent circuit (inset). R_1 is the resistance of the tunneling junction between source and Au NP (junction 1), C_1 is the capacitance of the junction 1, R_2 is the resistance of the tunneling junction between Au NP and drain (junction 2), C_2 is the capacitance of the junction 2. C_{g1} (C_{g2}) is the gate capacitances between side gate 1 (2) and Au NP. (b) Schematic illustration of an SET in which a gold nanoparticle is chemisorbed between the nanogap electrodes.

modulation of each side gate at a temperature of 9 K. Further, we plotted the experimentally determined tunneling current (I) of the device as a function of the drain voltage (V_d) and the bias voltage of side gate 1 (hereafter gate 1) (V_{g1}), which is the so-called stability diagram (see Figure 2a). Figure 2b shows the experimental stability diagram for the voltage of side gate 2 (hereafter gate 2) (V_{g2}). Both these stability diagrams show Coulomb blockade regions (Coulomb diamonds) present at regular intervals along the lateral axis, where the heights of all diamonds in a particular diagram were nearly equal, as were the widths. Figure 2 panels c and d show the differential conductances (dI/dV_d) of these stability diagrams, derived by the numerical differentiation of the plots in Figure 2 panels a and b, respectively, where we can see the Coulomb diamonds more clearly. In Figure 2c,d, the stability diagrams in the dI/dV_d plots exhibit simple periodic patterns of Coulomb diamonds against V_{g1} and V_{g2} axes. It notes that, if plural NPs are introduced between nanogap electrodes, these simple periodic Coulomb diamonds are not observed. In the experiments, we prepared 157 SETs on the substrate. Fourteen perecent of SETs (22 out of 157 SETs) showed the Coulomb diamonds based on the single NP as the Coulomb island.

From the slope of the Coulomb diamond in the dI/dV_d plot, we estimated the following: C_1 = 1.36 aF, C_2 = 1.22 aF, C_{g1} = 0.028 aF, and C_{g2} = 0.038 aF; from these values, the charging energy[20] is given as $E_C = e^2/2(C_1 + C_2 + C_{g1} + C_{g2})$ = 30 meV. It is noteworthy that the C_1 and C_2 values estimated from the stability diagram of V_{g1} are identical to those of V_{g2}. On account of the geometrical layout of the Au NP (Coulomb island), the source/drain electrodes, and gate $^1/_2$ electrodes, the capacitance of gate 1 (C_{g1}) differs slightly from that of gate 2 (C_{g2}). However, C_{g1} and C_{g2} are sufficient to achieve a logic operation under bias voltages of the two input gates. Figure 2e shows the experimentally determined $I-V_d$ characteristics for V_{g2} of 0.85, 1.90, and 2.95 V (solid lines). For comparison, this figure also shows theoretical $I-V_d$ curves obtained by the Orthodox theory at different values of fractional charge (Q_0), from which we get R_1 = 10 MΩ and R_2 = 510 MΩ.[21−23] V_{g2} values of 0.85, 1.90, and 2.95 V correspond to Q_0 values of $e/2$, $e/4$, and 0, respectively (dashed lines). Q_0 is calculated as $-0.3e$ (=(2.95 V) × C_{g2}/e − 1). It notes that the value of Q_0 is very stable and maintained through all of the experiments. The fairly good agreement between the theoretically and experimentally determined curves also suggests that the single Au NP contributes to the current flow between the source and drain electrodes. As R_2 is much larger than R_1 (R_2/R_1 = 51), the $I-V_d$ characteristic becomes asymmetric at V_{g2} = 1.9 V around V_d = 0 as shown in Figure 2e. The onsets of a step increase and a linear increase in current were observed at negative and positive voltages, and have been explained by the change in the excess number of electrons on the NP (N) and the overcoming the Coulomb blockade of C_1, respectively.[21−23]

Figure 2f shows the experimental $I-V_{g2}$ characteristics for the V_d values indicated by the horizontal arrows in Figure 2b; we can see the ideal Coulomb oscillation in Figure 2f. An asymmetric Coulomb oscillation peak is observed. The steep positive slope and the gradual negative slope are also explained as the change in N and the overcoming the Coulomb blockade of C_1, respectively.[21−23] It has been reported that an SET having only one metallic Coulomb island can exhibit ideal Coulomb oscillations, where a constant on-current flows periodically and the off-current (*i.e.*, 0 A) owing to the Coulomb blockade also flows periodically.[24−27] However, this is not the case with SETs fabricated using silicon technology[9−11] or CNTs[4,12] or with SETs containing multiple Coulomb islands, since these islands contribute to the tunneling process.[28−30]

The electrical properties of the SET as shown in Figure 2 remain stable for over a week, which implies that its tunneling parameters, that is, R_1, R_2, and Q_0, are extremely stable at 9 K. If the charge were to be trapped around the Coulomb island during the measurement, the stability diagram would not be observed clearly. As shown in Figure 2c,d, Q_0 of the Au NP varies with V_{g1} and V_{g2} without any distortion or hysteresis within the gate voltage range of −8 to 8 V. Such exceptionally stable properties are one of the key advantages of our chemically assembled SETs. This stability is explained as follows. The surface of the electrodes is covered with alkanethiol SAMs; alkanethiol also constitutes the ligand molecules of the Au NP, and the Au NP is chemisorbed to the source and drain electrodes by alkanedithiol molecules. Furthermore, the two tunneling barriers between the Au core of the NP and the

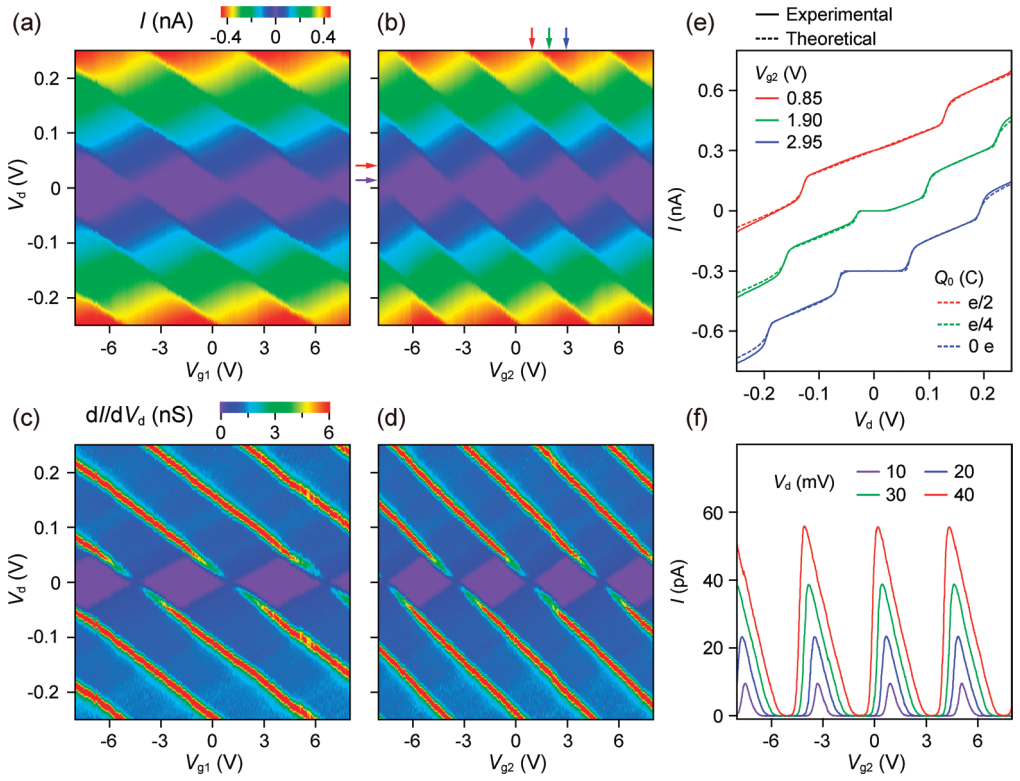

Figure 2. Plot of output current as a function of drain voltage and voltage of (a) side gate 1 or (b) side gate 2, at 9 K. Panels c and d show differential conductance plots derived from panels a and b, respectively, by numerical derivation. (e) Experimentally determined $I-V_d$ curves for different voltages of side gate 2 indicated by the vertical arrows in panel b (solid lines). The dashed lines show theoretical $I-V_d$ curves obtained by a conventional theory at different values of fractional charge (Q_0). (f) $I-V_{g2}$ curves for different drain voltages indicated by the horizontal arrows in panel b.

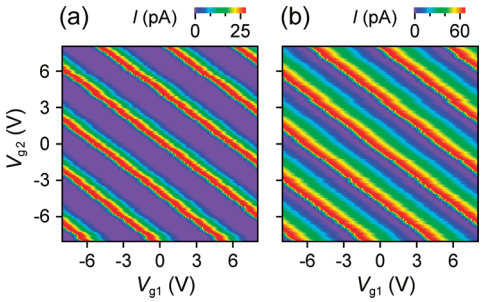

Figure 3. Plot of 2D output current *versus* bias voltages of side gates 1 and 2, at drain biases (V_d) of (a) 25 and (b) 45 mV.

source/drain electrodes are made of alkanethiol and alkanedithiol molecules. These alkanethiol and alkanedithiol molecules are stable as electrical insulating materials, because of which the formed Coulomb diamonds exhibit ideal properties without any distortions or hysteresis (Figure 2). Then, because of this advantage, we were able to thoroughly measure the SET properties and demonstrate the logic operation, as described below.

In the double-gate SET, the phase of the Coulomb oscillation shifts with a change in V_{g1} and V_{g2} individually. Figure 3 panels a and b show experimental 2D-output current characteristics of the double-gate SET as a function of V_{g1} for different V_{g2} at drain biases of 25 and 45 mV, respectively. In these two figures, the areas shaded in purple and other colors correspond to the regions in which Coulomb blockade is maintained (corresponding to device stability) and broken, respectively. On the basis of the oblique pattern of the rainbow stripes as seen in the 2D-output current characteristics, the phase of the Coulomb oscillation is expressed by a linear combination of V_{g1} and V_{g2}. The slope of the rainbow stripes is given by the ratio C_{g1}/C_{g2},[9] and is estimated as 0.74. As shown in Figure 3b, this ratio is independent of V_d (25 and 45 mV). The stability regions for $V_d = 45$ mV are smaller than those for $V_d = 25$ mV, which is also in agreement with the conventional theory.

The 2D-output current characteristics of the double-gate SET enable the various logic operations. As shown in Figure 2, C_{g1} and C_{g2} are estimated as 0.028 and 0.038 aF, respectively, and the Coulomb oscillation spacing for ΔV_{g1} ($=e/C_{g1}$) and ΔV_{g2} ($=e/C_{g2}$) are 5.7 and 4.2 V, respectively. Figure 4a shows the 2D-output current characteristics at $V_d = 30$ mV. From this figure, it can be seen that the maximum current (red regions) of 37 pA flows at (V_{g1}, V_{g2}) of (0, 0.40 V); this current corresponds to the point when the normalized linear combination of the bias voltages of both gates, m ($= V_{g1}/\Delta V_{g1} + (V_{g2} - V_{g2}')/\Delta V_{g2}$), becomes an integer, where V_{g2}' is 0.40 V. This maximum current also flows when (V_{g1}, V_{g2}) becomes ($\Delta V_{g1}/2$, $V_{g2}' + \Delta V_{g2}/2$), since

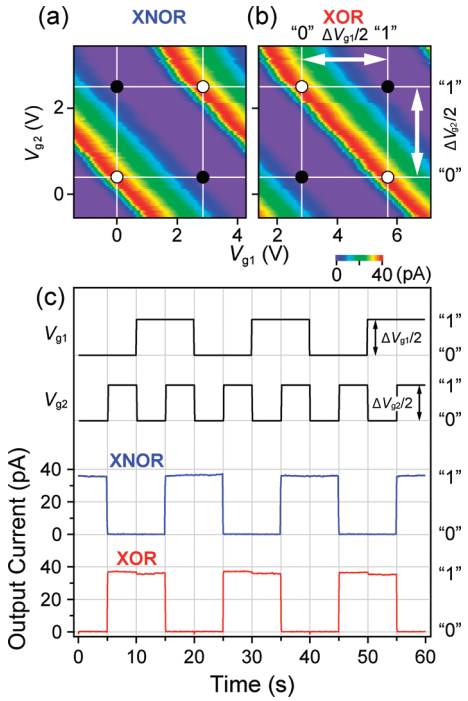

Figure 4. Plot of 2D output current for half Coulomb oscillation squares *versus* V_{g1} and V_{g2} for (a) XNOR and (b) XOR operations at V_d = 30 mV. The open circles (37 pA) and closed circles (0.2 pA or less) represent the combination of the gate operation points. (c) The logic operation of XNOR and XOR gates for two input pulses. In the case of XNOR operation, the height of the input pulse voltage for gate 1 (2) is $\Delta V_{g1}/2$ ($\Delta V_{g2}/2$) and the origin point (both input levels are low ("0")) of (V_{g1}, V_{g2}) is (0, 0.40 V). In the case of XNOR operation, the origin point of (V_{g1}, V_{g2}) is ($\Delta V_{g1}/2$, 0.40 V), and the height of the input pulse voltage for gate 1 (2) is $\Delta V_{g1}/2$ ($\Delta V_{g2}/2$).

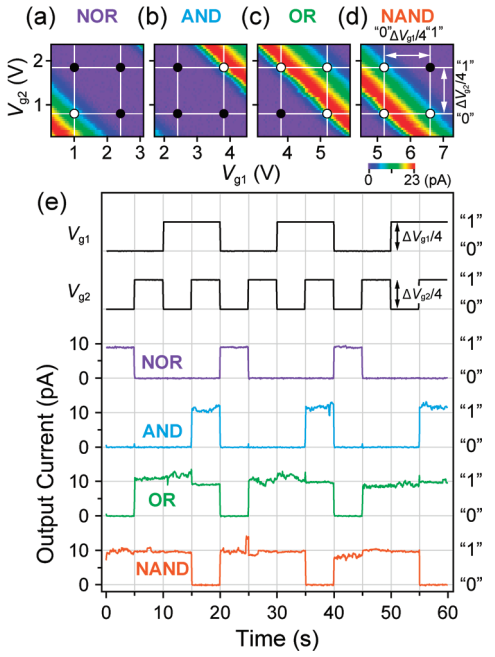

Figure 5. Plot of 2D output current for quarter Coulomb oscillation squares *versus* V_{g1} and V_{g2} for (a) NOR, (b) AND, (c) OR, and (d) NAND operations at V_d = 20 mV. The open circles (10 pA) and closed circles (0.2 pA or less) represent the combination of the gate operation points. (e) Logic operation of NOR, AND, OR, NAND gates for two input pulses. The height of the input pulse for gate 1 (2) is $\Delta V_{g1}/4$ ($\Delta V_{g2}/4$). In the cases of the NOR, AND, OR, and NAND operations, the origin point of V_{g1} is shifted $\Delta V_{g1}/4$ one by one and V_{g2} is a constant value of 0.80 V.

m becomes 1. On the contrary, *m* becomes 0.5 at (V_{g1}, V_{g2}) = (0, $V_{g2}' + \Delta V_{g2}/2$) or ($\Delta V_{g1}/2$, V_{g2}'), which corresponds to the condition of Coulomb blockade being unbroken (purple area in Figure 4a) and an output current of 0.

The XNOR operation is achieved by applying the combination of two V_{g1} input levels, 0 V and $\Delta V_{g1}/2$ as "0" and "1," and two V_{g2} input levels, V_{g2}' and $V_{g2}' + \Delta V_{g2}/2$ as "0" and "1," respectively, which is the half Coulomb oscillation square of (V_{g1}, V_{g2}) (see white square in Figure 4a). This operation is shown in Figure 4c (blue solid line); here, the (V_{g1}, V_{g2}) input levels of (0, 0) and (1, 1) give an "on" current of 37 pA, and (V_{g1}, V_{g2}) of (0, 1) and (1, 0) give an "off" current of 0.2 pA or less. It can be seen that the on/off current ratio is more than 10^2.

The XOR operation is achieved by applying the next half Coulomb oscillation square against V_{g1}, that is, two V_{g1} input levels of $\Delta V_{g1}/2$ and ΔV_{g1} as "0" and "1" and two V_{g2} input levels of V_{g2}' and $V_{g2}' + \Delta V_{g2}/2$ as "0" and "1," respectively (red solid line in Figure 4c). It can be seen that the on/off current ratio for the XOR operation is the same as that for the XNOR operation, 10^2; the reason for being is that the double-gate SET exhibits ideally periodic Coulomb oscillation against V_{g1} and V_{g2}. These on/off ratios are larger than that of double-gate SETs fabricated by using silicon technology[9−11] or a CNT.[12]

The high periodicity of Coulomb oscillations of the fabricated double-gate SET enables not only the XNOR and XOR operations but also other two-input logic operations such as NOR, AND, OR, and NAND. The output current of 10 pA can be generated at V_d = 20 mV by using both the positive and the negative slopes of a Coulomb oscillation peak with changing $\Delta V_{g1}/4$ and $\Delta V_{g2}/4$, as shown in Figure 2.

Figure 5 panels a−d demonstrate NOR, AND, OR, and NAND operations by using quarter Coulomb oscillation squares. In Figure 5d, the NAND operation is explained as follows: Here, (V_{g1}'', V_{g2}'') of (5.2 V, 0.80 V) is taken as the origin of the input levels of (0, 0). Changing (V_{g1}, V_{g2}) to three-quarter Coulomb oscillation squares (V_{g1}'', V_{g2}''), ($V_{g1}'' + \Delta V_{g1}/4$, V_{g2}''), and (V_{g1}'', $V_{g2}'' + \Delta V_{g2}/4$), corresponding to (0, 0), (1, 0), and (0, 1), respectively, results in an output current of 10 pA (on state). On the contrary, at ($V_{g1}'' + \Delta V_{g1}/4$, $V_{g2}'' + \Delta V_{g2}/4$) of (1, 1), the output current becomes 0.2 pA or less (off state), i.e., the NAND operation. Figure 5e shows the actual output current for the NAND operation for two input pulses (orange solid line), where the height and offset of the input pulse are $\Delta V_{g1}/4$ and V_{g1}'' for gate 1 and $\Delta V_{g2}/4$ and V_{g2}'' for gate 2, respectively.

Figure 5 panels a–c show the next three-quarter Coulomb oscillation squares against V_{g1}, where the origins of the input levels are ($V_{g1}'' - 3\Delta V_{g1}/4$, V_{g2}''), ($V_{g1}'' - 2\Delta V_{g1}/4$, V_{g2}''), and ($V_{g1}'' - \Delta V_{g1}/4$, V_{g2}''), respectively; accordingly, the logic operations of the fabricated two-gate SET become NOR, AND, and OR, respectively, from the NAND operation. Figure 5e also shows the output currents for the NOR, AND, and OR operations for two input pulses (purple, blue, and green solid lines, respectively); here, the heights of the input pulses for gates 1 and 2 are $\Delta V_{g1}/4$ and $\Delta V_{g2}/4$, respectively. The levels of output current in the off states for NOR, AND, OR, and NAND are the same as those for XNOR and XOR—0.2 pA or less. This observation indicates that our fabricated SET can have versatile logic operations with the same output property. These logic operations are expected to be available at room temperature if we use smaller NPs such as 2 nm in the core diameter.[23] For the ideal logic operations, the gate-capacitance ratio of C_{g1}/C_{g2} should be 1. In the present experiment, it is 0.74. As the value of the gate capacitance strongly depends on the SET structures consisting of NP, source/drain electrodes and two side gate electrodes, the shape of nanogap electrodes is a key issue to obtain the gate-capacitance ratio of 1. As the position of NP is almost center of nanogap electrodes in the present SET, the gate-capacitance ratio will be improved by narrowing the width of the nanogap electrodes.

CONCLUSION

We have chemically assembled double-gate SET by using electroless gold-plated nanogap electrodes and chemisorbed chemically synthesized gold nanoparticles. The SET exhibits more than three cycles of Coulomb diamonds under changing bias voltages of both the gates without any distortion or hysteresis, and the electron transfer properties of the SET are highly stable during the operation period (more than a week) at 9 K. Phase shift of the Coulomb oscillation according to a linear combination of the gate voltages gives XOR and XNOR operations with an on/off current ratio of 10^2. Furthermore, the NAND, OR, NOR, and AND operations are achieved using the same SET. Owing to the stability of the fabricated SET, it is expected to be useful in applications requiring versatile logic gate operations with high precision and stability.

METHODS

The overall chemical assembling processes of SET fabrication are shown in the previous reports.[13–15] Preliminary source and drain electrodes with two side gates were fabricated on a Si/SiO_2 substrate by electron beam lithography (EBL) and lift-off, with the gap between the source and the drain kept at ~25 nm. Although these preliminary electrodes were prepared by the top-down approach of EBL, subsequent fabrication was done using the bottom-up approach, wherein the SET was fabricated only to immerse the substrate into various solutions. The nanogap electrodes were then fabricated by electroless gold plating using iodine tincture,[19] where the gap was controlled by tuning the plating time. In this study, we maintained a gap of about 10 nm between the source and drain electrodes (see Figure 1a); this gap is large enough for introducing into it a decanethiol-protected Au NP with diameter of about 9 nm (core diameter of 6.2 ± 0.8 nm), which was chemically synthesized.[16] A Coulomb island was introduced in the following three steps: (1) an octanethiol self-assembled monolayer (SAM) was formed on the surface of the electrodes, (2) decanedithiol was introduced into the SAM, and (3) the decanethiol-protected Au NP was chemisorbed *via* decanedithiol (see Figure 1b).[17,18]

Experimental setup measuring electron transport properties of SET is also same as the previous work.[15]

Conflict of Interest: The authors declare no competing financial interest.

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